The documentation and process conversion measures necessary to comply with this revision shall be completed by 25 May 2016.

INCH-POUND

MIL-PRF-19500/744E
25 February 2016
SUPERSEDING
MIL-PRF-19500/744D
4 January 2013

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, FIELD EFFECT, N-CHANNEL,
RADIATION HARDENED, LOGIC-LEVEL SILICON,
ENCAPSULATED (SURFACE MOUNT PACKAGE), TYPES 2N7616,
QUALITY LEVELS JANTXV AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for a N-channel, enhancement-mode, radiation hardened (total dose and single event effects (SEE)), low-threshold logic level, MOSFET, transistor. Two levels of product assurance (JANTXV and JANS) are provided for each encapsulated device with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). Provisions for radiation hardness assurance (RHA) to two radiation levels ("R" and "F") are provided for JANTXV and JANS product assurance levels. See 6.7 for JANHC and JANKC die versions.

* 1.2 Package outlines. The device package outlines are as follows: UB, UBC, UBCN and UBN in accordance with figure 1 for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Type	P_T T_A = +25°C (1)	P_T (infinite sink) T_{IS} = +25°C	$R_{\theta JA}$ (2)	V_{DS}	V_{GS}	I_{D1} T_C = +25°C (3) (4)	I_{D2} T_C = +100°C (3) (4)	I_S	I_{DM} (5)	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	A dc	A dc	A dc	A (pk)	°C
2N7616UB, UBC, UBN, UBCN	0.62	1.25	200	60	±10	0.8	0.5	0.8	3.2	-55 to +150

(1) Derate linearly by 4.5 mW/°C for T_A > +25°C
(2) See figure 2, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D limit:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 3, maximum drain current graph.
(5) I_{DM} = 4 X I_{D1} as calculated in note (3).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

1.4 Maximum ratings. Unless otherwise specified, T_C = +25°C.

Type	Min $V_{(BR)\ DSS}$ V_{GS} = 0 V I_D = 250 µA dc	$V_{GS\ (th)1}$ V_{DS} = V_{GS} I_D = 250 µA dc	Max I_{DSS1} V_{GS} = 0 V V_{DS} = 80% rated VDS	Max $r_{DS(on)}$ (1) V_{GS} = 4.5 V dc		E_{AS}	I_{AS}
				at I_{D2} T_J = +25°C	T_J = +150°C		
	V dc	V dc Min Max	µA dc	Ohm	Ohm	mJ	A dc
2N7616UB UBC, UBN, UBCN	60	1.0 2.0	1.0	0.680	1.020	26.6	1.0

(1) Pulsed (see 4.5.1).

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: “JANTXV” and "JANS".

* 1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "R" and "F".

* 1.5.3 JAN brand and quality level designators for unencapsulated devices (die). See 6.7 for unencapsulated devices.

* 1.5.4 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.4.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

* 1.5.4.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7616".

* 1.5.4.3 Suffix letters. The following suffix letters are incorporated in the PIN for this specification sheet:

UB	Indicates a 4-pad, Metal Lid (Shield) connected to 4th pad
UBC	Indicates a 4-pad, Ceramic Lid, lid braze ring connected to 4th pad
UBN	Indicates a 3-pad, Isolated Metal Lid
UBCN	Indicates a 3-pad, Isolated Ceramic Lid

* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

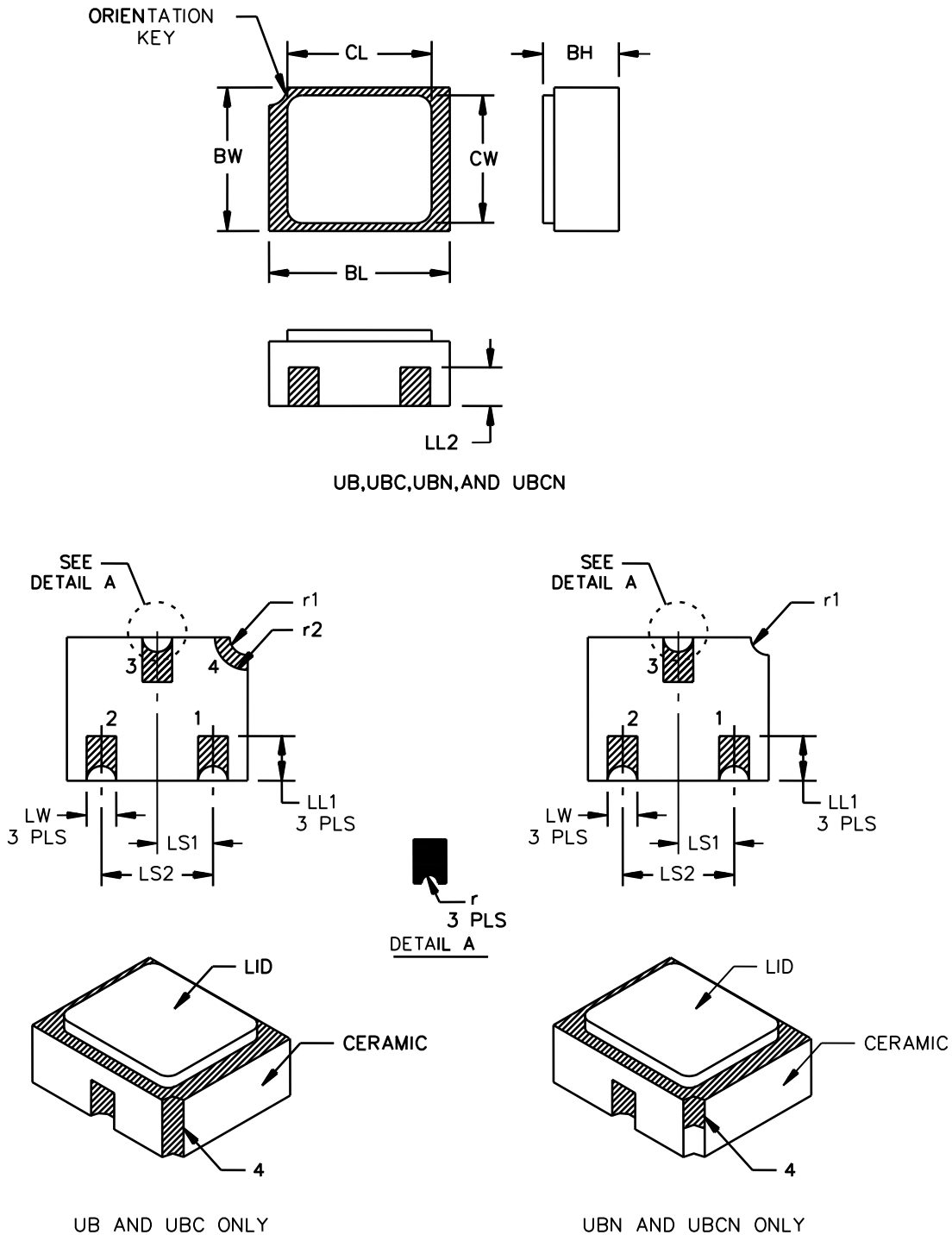


FIGURE 1. Physical dimensions, surface mount (UB, UBN, UBC and UBCN versions).

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.115	.128	2.92	3.25	
BW	.095	.108	2.41	2.74	
BH	.046	.056	1.17	1.42	UB only, 4
BH	.046	.056	1.17	1.42	UBN only, 5
BH	.055	.069	1.40	1.75	UBC only, 6
BH	.055	.069	1.40	1.75	UBCN only, 7
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.97	3 PLS
LL2	.014		0.356		3 PLS
LS_1	.035	.039	0.89	0.99	
LS_2	.071	.079	1.80	2.01	
LW	.016	.024	0.41	0.61	
r		.008		0.20	6
r1		.012		0.30	8
r2		.022		0.56	UB & UBC only, 8

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas.
4. UB only: Pad 1 = Gate, Pad 2 = Source, Pad 3 = Drain, Pad 4 = Shielding connected to the metal lid.
5. UBN only: Pad 1 = Gate, Pad 2 = Source, Pad 3 = Drain, Isolated lid with 3 pads only.
6. UBC (ceramic lid) only: Pad 1 = Gate, Pad 2 = Source, Pad 3 = Drain, Pad 4 = Connected to the lid braze ring.
7. UBCN (ceramic lid) only: Pad 1 = Gate, Pad 2 = Source, Pad 3 = Drain, Isolated lid with 3 pads only.
8. For design reference only.
9. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions, surface mount (UB, UBN, UBC and UBCN versions) - Continued.

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

I_{AS} ..... Rated avalanche current, nonrepetitive
nC ..... nano Coulomb.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500 and figure 1 (UB, UBN, UBC and UBCN) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Internal construction. Multiple chip construction shall not be permitted.

* 3.5 Marking. Marking shall be in accordance with MIL-PRF-19500. Marking on the UB package shall consist of an abbreviated part number, the date code, and the manufacturer’s symbol or logo. The prefixes JANTXV and JANS can be abbreviated as JV and JS respectively. The "2N" prefix and the "UB" suffix can also be omitted. The radiation hardened designator R or F, shall immediately precede (or replace) the device “2N” identifier (depending upon degree of abbreviation required).

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

a. Devices shall be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100$ kΩ, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.8 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of Inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I, II, and III).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 SEE. SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with table II. SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS	JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
9	Subgroup 2 of table I herein I_{DSS1}, I_{GSSF1}, I_{GSSR1} as minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein. ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±0.2 µA dc or ±100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±0.2 µA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.	Subgroup 2 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±0.2 µA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and $V_{GS(th)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a. JANTXV level does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 15 V minimum for t = 250 μs minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current (I_{AS}).....1.0 A.

b. Peak gate voltage (V_{GS}).....10 V dc (up to max rated V_{GS}).

c. Gate to source resistor (R_{GS}).....$25 \leq R_{GS} \leq 200\ \Omega$.

d. Initial case temperature .....+25°C, +10°C, -5°C.

e. Inductance: ..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

f. Number of pulses to be applied .....1 pulse minimum.

g. Supply voltage (V_{DD}).....25 V dc (up to max V_{DS}).

* 4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). See table III, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein. Electrical measurements (end-points) shall be in accordance with the inspections of table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and herein.

* 4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1051	Test condition G, 100 cycles.
B3	2077	SEM.
B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated V_{GS}; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated V_{DS}; T_A = +175°C, t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.
B5	2037	Test condition D.

* 4.4.2.2 Quality levels JAN, JANTX and JANTXV, table E-VIB of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition C, 25 cycles.
* B3	1042	Intermittent operation life, condition D.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

Subgroup	Method	Condition
C2	2036	Terminal strength is not applicable.
C5	3161	See 4.3.3, $R_{\theta JA}$ = (see 1.3).
* C6	1042	Intermittent operation life, condition D.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

* 4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JA}$			°C/W
Breakdown voltage drain to source	3407	V_{GS} = 0, I_D = 250 µA dc, bias condition C	$V_{(BR)DSS}$	60		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 250 µA dc	$V_{GS(TH)1}$	1.0	2.0	V dc
Gate current	3411	V_{GS} = +10 V dc, bias condition C, V_{DS} = 0	I_{GSSF1}		+100	nA dc
Gate current	3411	V_{GS} = -10 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		-100	nA dc
Drain current	3413	V_{GS} = 0, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS1}		1.0	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 4.5 V dc, condition A, pulsed (see 4.5.1), I_D = I_{D2}	$r_{DS(ON)1}$		0.680	Ω
Forward voltage	4011	V_{GS} = 0, condition A, pulsed (see 4.5.1), I_D = I_{D1}	V_{SD}		1.2	V (pk)
Subgroup 3						
High temperature operation:		T_C = T_J = +125°C				
Gate current	3411	V_{GS} = ±10 V dc, bias condition C, V_{DS} = 0	I_{GSS2}		±200	nA dc
Drain current	3413	V_{GS} = 0, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		10	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 4.5 V dc, condition A, pulsed (see 4.5.1), I_D = I_{D2}	$r_{DS(ON)2}$		0.980	Ω
Gate to source voltage (threshold)	3403	V_{DS} = V_{GS}, I_D = 250 µA dc	$V_{GS(TH)2}$	0.5		V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 3 – Continued.						
Low temperature operation:		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 250$ µA dc	$V_{GS(TH)3}$		2.5	V dc
Subgroup 4						
Forward transconductance	3475	$V_{DS} = 10$ V dc, $I_D = I_{D2}$, pulsed (see 4.5.1)	g_{FS}	0.23		S
Gate series resistance	3402	Condition B	R_G		14	Ω
Subgroup 5						
Safe operating area test	3474	V_{DS} = 80 percent of rated V_{DS} (see 1.3); $t_P = 10$ ms, I_D as specified on figure 4				
Electrical measurements		See table I, subgroup 2				
Subgroups 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B, $I_D = I_{D1}$, V_{DD} = 50 percent rated V_{DS}				
On-state gate charge			$Q_{G(on)}$		3.6	nC
On gate to source charge			Q_{GS1}		1.5	nC
On gate to drain charge			Q_{GD1}		1.8	nC
Turn-off gate charge			$Q_{G(off)}$		3.6	nC
Off gate to source charge			Q_{GS2}		1.5	nC
Off gate to drain charge			Q_{GD2}		1.8	nC
Reverse recovery time	3473	di/dt = -100 A/µs, $V_{DD} \leq 25$ V, $I_D = I_{D1}$	t_{rr}		78	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ This test required for the following end-point measurements only:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

* TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Post-irradiation limits		Unit
				R and F		R		F		
	Method	Conditions		Min	Max	Min	Max	Min	Max	
Subgroup 1										
Not applicable										
Subgroup 2		T_C = + 25°C								
Steady-state total dose irradiation (V_{GS} bias) 4/	1019	V_{GS} = 10 V; V_{DS} = 0								
Steady-state total dose irradiation (V_{DS} bias) 4/	1019	V_{GS} = 0; V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	V_{GS} = 0; I_D = 250 µA; bias condition C	$V_{(BR)DSS}$	60		60		60		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ I_D = 250 µA	$V_{GS(th)1}$	1.0	2.0	1.0	2.0	1.0	2.0	V dc
Gate current	3411	V_{GS} = +10 V, V_{DS} = 0, bias condition C	I_{GSSF1}		100		100		100	nA dc
Gate current	3411	V_{GS} = -10 V, V_{DS} = 0, bias condition C	I_{GSSR1}		-100		-100		-100	nA dc
Drain current	3413	V_{GS} = 0, bias condition C; V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)	I_{DSS}		1.0		1.0		1.0	µA dc
* Static drain to source on-state voltage	3405	V_{GS} = 4.5 V; condition A, pulsed (see 4.5.1), $I_{D1} = I_{D2}$	$V_{DS(on)}$		0.34		0.34		0.34	V dc
Forward voltage source drain diode	4011	V_{GS} = 0; I_D = I_{D1} bias condition C	V_{SD}		1.2		1.2		1.2	V dc

1/ For sampling plan see MIL-PRF-19500.
2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheets utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
4/ Separate samples shall be pulled for each bias.

TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	Condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2	
Subgroup 2 1/			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Subgroup 3			45 devices c = 0
Switching time test	3472	$I_D = I_{D1}$, V_{GS}= 5.0 V dc, R_G = 24Ω, V_{DD} = 50 percent rated V_{DS} Maximum measurements: $t_{d(on)}$ = 8 ns; t_r = 24 ns; $t_{d(off)}$ = 30 ns; t_f = 13 ns	
Subgroup 4			Sample size N/A
Thermal impedance curves	3161	See MIL-PRF-19500.	
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	
Subgroup 11			3 devices
SEE 2/ 3/	1080	See MIL-STD-750 method 1080 and 6.2.	

1/ A separate sample for each test shall be pulled.
2/ Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

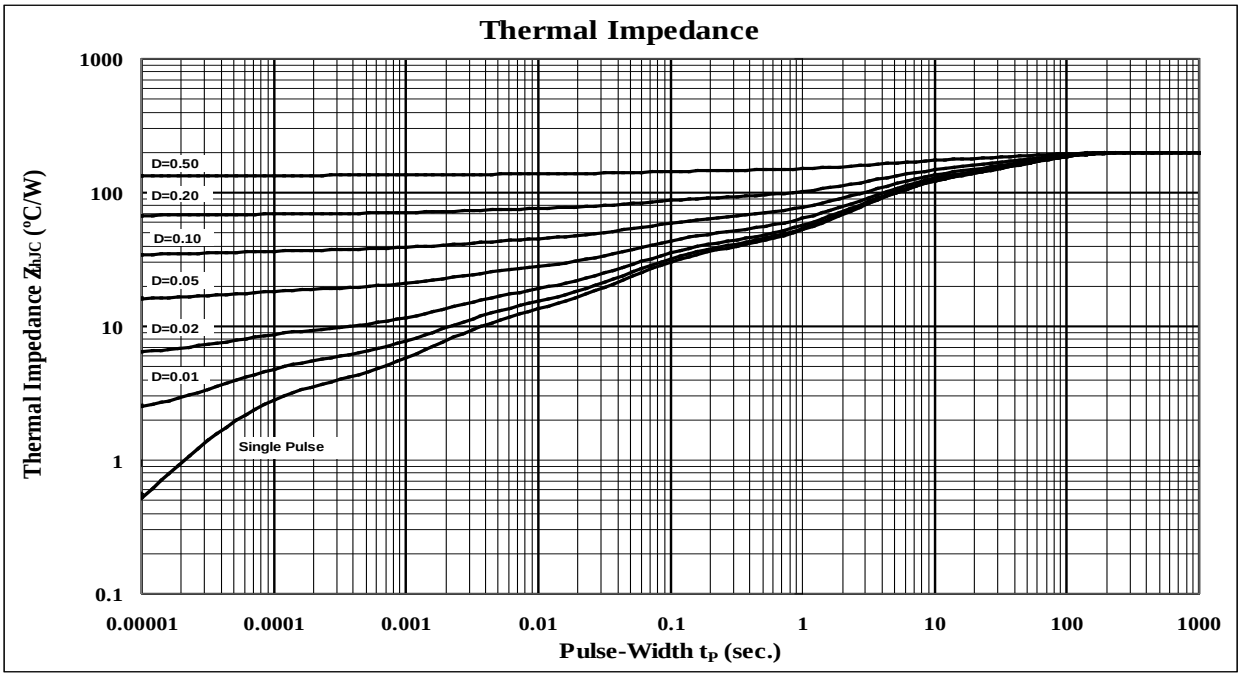


FIGURE 2. Thermal impedance graph.

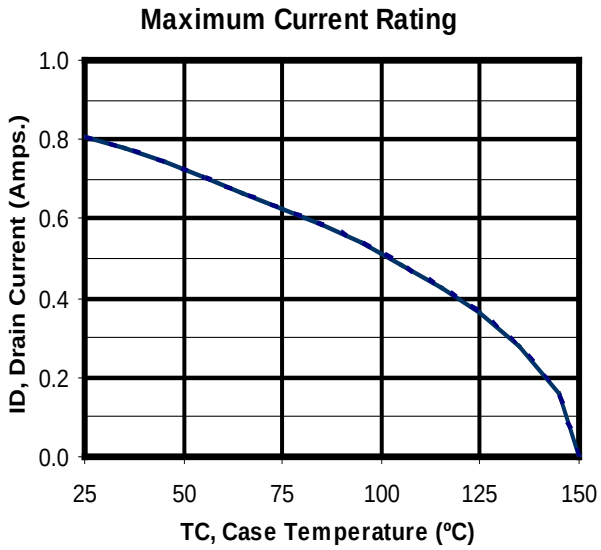


FIGURE 3. Derating drain current .

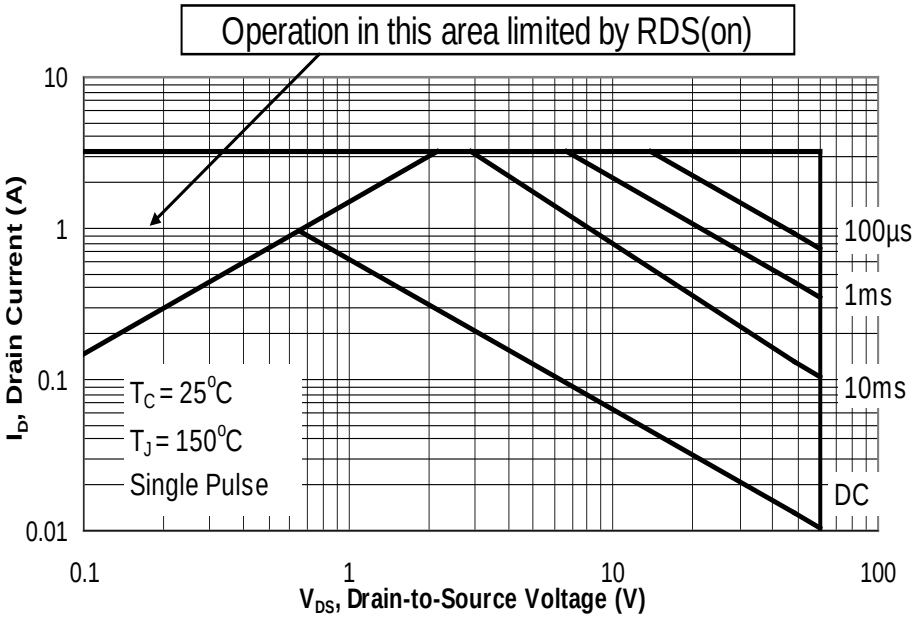


FIGURE 4. Safe-operating-area graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

* d. The complete PIN, see 1.5 and 6.5.

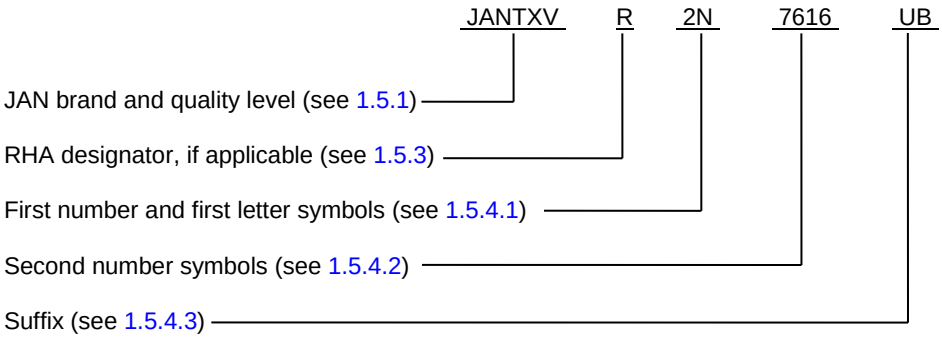
e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract or order.

f. If specific SEE characterization conditions are desired (see section 6.8 and table IV), manufacturer's cage code should be specified in the contract or order.

g. If SEE testing data is desired, it should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

* 6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



* 6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7616UB	JANTXV#2N7616UB	JANS2N7616UB	JANS#2N7616UB
JANTXV2N7616UBC	JANTXV#2N7616UBC	JANS2N7616UBC	JANS#2N7616UBC
JANTXV2N7616UBCN	JANTXV#2N7616UBCN	JANS2N7616UBCN	JANS#2N7616UBCN
JANTXV2N7616UBN	JANTXV#2N7616UBN	JANS2N7616UBN	JANS#2N7616UBN

(1) The number sign (#) represent one of two RHA designators available on this specification sheet (“R” or "F").

6.6 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N	Package & Termination Configuration
IRHLUB770Z4	2N7616UB	4-pad, Metal Lid (Shield) connected to 4th pad
IRHLUBN770Z4	2N7616UBN	3-pad, Isolated Metal Lid
IRHLUBC770Z4	2N7616UBC	4-pad, Ceramic Lid, lid braze ring connected to 4th pad
IRHLUBCN770Z4	2N7616UBCN	3-pad, Isolated Ceramic Lid

6.7 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/741.

6.8 Application data.

6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see table IV) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

TABLE IV. Manufacturers characterization conditions.

Manufacture s cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of 21 August 2012 and older)	SEE 1/	1080	See MIL-STD-750E method 1080.0 dated 20 November 2006. See figure 5	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	3 devices
	SEE irradiation:		Fluence = 3E5 ±20 percent ions/cm^2 Flux = 2E3 to 2E4 ions/cm^2/sec, temperature = 25º ±5 °C Surface LET = 38 MeV-cm^2/mg ±5.0 %, range = 38 µm ±7.5%, energy = 300 MeV ±7.5% (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator) In-situ bias conditions: V_{DS} = 60 V and V_{GS} = -6 V V_{DS} = 35 V and V_{GS} = -7 V Surface LET = 62 MeV-cm^2/mg ±5.0 %, range = 33 µm ±7.5%, energy = 355 MeV ±7.5% (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator) In-situ bias conditions: V_{DS} = 60 V and V_{GS} = -5 V V_{DS} = 30 V and V_{GS} = -6 V Surface LET = 85 MeV-cm^2/mg ±5 %, range = 29 µm ±7.5%, energy = 380 MeV ±10% (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator) In-situ bias conditions: V_{DS} = 60 V and V_{GS} = -4 V V_{DS} = 40 V and V_{GS} = -5 V	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
Upon qualification, all manufacturers shall provide the verification test conditions to be added to this table.				

1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

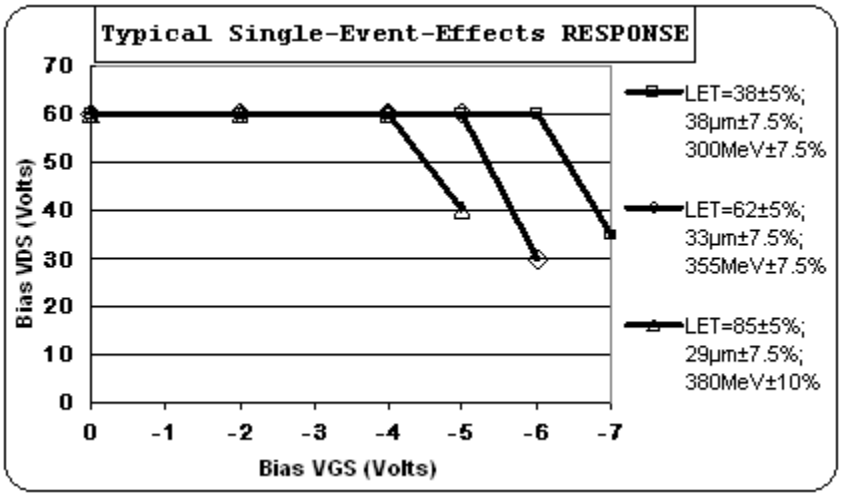


FIGURE 5. Cage 68210 typical SEE response graph.

* 6.9 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218–3990 or by electronic mail at Semiconductor@.dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

6.10 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2016-023)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.